	L #	Hits	Search Text	DBs
1	L1	4180	(sequenc$3 issu$3 dispatch$3) near10 instruction near20 ((composite comput$5 process$3 operation$3 function$3) adj2 (block unit module engine subunit element subsystem))	USPAT; US-PGPUB
2	L2	455796	(status state condition) near10 (network rout$3 bus connect$3 interconnect$3 path line)	USPAT; US-PGPUB
3	L3	7078	2 near20 ((composite comput$5 process$3 operation$3 function$3) adj2 (block unit module engine subunit element subsystem))	USPAT; US-PGPUB
4	L4	522	1 and 3	USPAT; US-PGPUB
5	L5	35351	((composite comput$5 process$3 operation$3 function$3) adj2 (block unit module engine subunit element subsystem)).ab,ti.	USPAT; US-PGPUB
6	L7	594	(sequenc$3 issu$3 dispatch$3) near10 instruction near20 ((composite comput$5 process$3 operation$3 function$3) adj2 (block unit module engine subunit element subsystem))	EPO; JPO; DERWENT; IBM_TDB
7	L8	277642	(status state condition) near10 (network rout$3 bus connect$3 interconnect$3 path line)	EPO; JPO; DERWENT; IBM_TDB
8	L9	2470	8 near20 ((composite comput$5 process$3 operation$3 function$3) adj2 (block unit module engine subunit element subsystem))	EPO; JPO; DERWENT; IBM_TDB
9	L11	15	7 and 9	EPO; JPO; DERWENT; IBM_TDB
10	L6	287	4 and 5	USPAT; US-PGPUB
11	L14	89	13 and @pd<19920610	USPAT; US-PGPUB
12	L15	218	(sequencer) near10 instruction near20 ((composite comput$5 process$3 operation$3 function$3) adj2 (block unit module engine subunit element subsystem))	USPAT; US-PGPUB
13	L16	12	3 and 15 not 6	USPAT; US-PGPUB
14	L19	332725	(status condition) near10 (communicat$3 transfer$4 network rout$3 bus connect$3 interconnect$3 path line)	USPAT; US-PGPUB
15	L20	4912	19 near20 ((composite comput$5 process$3 operation$3 function$3) adj2 (block unit module engine subunit element subsystem))	USPAT; US-PGPUB
16	L22	186252	(status condition) near10 (communicat$3 transfer$4 network rout$3 bus connect$3 interconnect$3 path line)	EPO; JPO; DERWENT
17	L23	1707	22 near20 ((composite comput$5 process$3 operation$3 function$3) adj2 (block unit module engine subunit element subsystem))	EPO; JPO; DERWENT; IBM_TDB
18	L24	1	7 and 23 not 11	EPO; JPO; DERWENT; IBM_TDB
19	L21	224	1 and 20 not 6	USPAT; US-PGPUB

	Document ID	U	Title	Current OR
1	US 20040049664 A1	☐	Methods and apparatus to support conditional execution in a VLIW-based array processor with subword execution	712/226
2	US 20040039899 A1	☒	Methods and apparatus to support conditional execution in a VLIW-based array processor with subword execution	712/226
3	US 20030149671 A1	☒	License information exchange system	705/59
4	US 20030115083 A1	☒	HTML-based clinical content	705/2
5	US 20030101200 A1	☒	Distributed file sharing system and a file access control method of efficiently searching for access rights	707/200
6	US 20030072263 A1	☒	Method and apparatus for monitoring and logging the operation of a distributed processing system	370/235
7	US 20030070059 A1	☒	System and method for performing efficient conditional vector operations for data parallel architectures	712/7
8	US 20030061601 A1	☒	Data processing apparatus and method, computer program, information storage medium, parallel operation apparatus, and data processing system	717/144
9	US 20030046402 A1	☒	Information processing apparatus and method, recording medium product, and program	709/228
10	US 20030007178 A1	☒	Information processing apparatus and control method therefor	358/1.15
11	US 20020188562 A1	☒	Billing system, and device constituting same	705/40
12	US 20020178345 A1	☒	Methods and apparatus to support conditional execution in a VLIW-based array processor with subword execution	712/24
13	US 20020087847 A1	☒	Method and apparatus for processing a predicated instruction using limited predicate slip	712/233
14	US 20020083173 A1	☒	Method and apparatus for optimizing selection of available contexts for packet processing in multi-stream packet processing	709/225
15	US 20020059908 A1	☒	Control system and method for operating an internal combustion engine	123/90.11
16	US 20020007450 A1	☒	Line-oriented reorder buffer	712/23
17	US 20010031150 A1	☒	Image forming apparatus capable of processing images of plural documents	399/82

	Document ID	U	Title	Current OR
18	US 20010016947 A1	☒	TV PLANNER FOR DSS	725/51
19	US 20010015815 A1	☒	IMAGE FORMING APPARATUS WHICH EXCELS IN REPRODUCIBILITY OF COLORS, FINE LINES AND GRADATIONS EVEN IN A COPY MADE FROM A COPIED IMAGE	358/1.9
20	US 6697878 B1	☒	Computer having a remote procedure call mechanism or an object request broker mechanism, and data transfer method for the same	719/316
21	US 6671762 B1	☒	System and method of saving and restoring registers in a data processing system	710/267
22	US 6567176 B1	☒	Information processing apparatus and control method therefor	358/1.14
23	US 6512899 B2	☒	Image forming apparatus capable of processing images of plural documents	399/82
24	US 6493819 B1	☒	Merging narrow register for resolution of data dependencies when updating a portion of a register in a microprocessor	712/210
25	US 6481010 B2	☒	TV planner for DSS	725/44
26	US 6453277 B1	☒	Virtual I/O emulator in a mainframe environment	703/24
27	US 6442627 B1	☒	Output FIFO data transfer control device	710/52
28	US 6435147 B1	☒	Control system and method for operating an internal combustion engine	123/90.11
29	US 6430646 B1	☒	Method and apparatus for interfacing a processor with a bus	710/305
30	US 6401219 B1	☒	Failure analysis system, method for managing estimated logic status and information storage medium for programmed instruction of the method	714/26
31	US 6393549 B1	☒	Instruction alignment unit for routing variable byte-length instructions	712/204
32	US 6388768 B2	☒	Image forming apparatus which excels in reproducibility of colors, fine lines and gradations even in a copy made from a copied image	358/1.9
33	US 6381689 B2	☒	Line-oriented reorder buffer configured to selectively store a memory operation result in one of the plurality of reorder buffer storage locations corresponding to the executed instruction	712/215
34	US 6366999 B1	☒	Methods and apparatus to support conditional execution in a VLIW-based array processor with subword execution	712/24
35	US 6356984 B1	☒	Digital data processing system having a data bus and a control bus	711/147
36	US 6351801 B1	☒	Program counter update mechanism	712/205
37	US 6347170 B1	☒	Miniature video in the guide logo	345/717
38	US 6348932 B1	☒	Provide two different types of service in a menu	345/719
39	US 6339592 B1	☒	Apparatus and method of connecting computer network to telephone	370/352

	Document ID	U	Title	Current OR
40	US 6311225 B1	☒	Method and apparatus for transferring data between process modules	719/310
41	US 6308250 B1	☒	Method and apparatus for processing a set of data values with plural processing units mask bits generated by other processing units	712/5
42	US 6298435 B1	☒	Methods and apparatus for exploiting virtual buffers to increase instruction parallelism in a pipelined processor	712/217
43	US 6298417 B1	☒	Pipelined cache memory deallocation and storeback	711/143
44	US 6269436 B1	☒	Superscalar microprocessor configured to predict return addresses from a return stack storage	712/23
45	US 6237082 B1	☒	Reorder buffer configured to allocate storage for instruction results corresponding to predefined maximum number of concurrently receivable instructions independent of a number of instructions received	712/215
46	US 6195744 B1	☒	Unified multi-function operation scheduler for out-of-order execution in a superscaler processor	712/215
47	US 6189089 B1	☒	Apparatus and method for retiring instructions in excess of the number of accessible write ports	712/218
48	US 6189068 B1	☒	Superscalar microprocessor employing a data cache capable of performing store accesses in a single clock cycle	711/3
49	US 6185565 B1	☒	System and method for communication session disposition responsive to events in a telecommunications network and the internet	707/10
50	US 6145049 A	☒	Method and apparatus for providing fast switching between floating point and multimedia instructions using any combination of a first register file set and a second register file set	710/267
51	US 6098167 A	☒	Apparatus and method for fast unified interrupt recovery and branch recovery in processors supporting out-of-order execution	712/218
52	US 5946489 A	☒	System for coupling a host computer to an image scanner in which high level functions are migrated to the attached host computer	710/5
53	US 5818454 A	☒	System for providing fast transfers to input/output device by assuring commands from only one application program reside in FIFO	710/37
54	US 5760835 A	☒	Window management system with recording status display	345/759
55	US 5353386 A	☒	Program counter update mechanism	712/205
56	US 5264782 A	☒	Recorder buffer and a method for allocating a fixed amount of storage for instruction results independent of a number of concurrently dispatched instructions	712/215
57	US 5023738 A	☒	Method and apparatus for accelerating the transfer of graphical images	710/23
58	US 5014234 A	☒	Superscalar microprocessor configured to predict return addresses from a return stack storage	712/23
59	US 4982324 A	☒	High performance superscalar alignment unit	712/204
60	US 4796167 A	☒	Range finding circuit for selecting a consecutive sequence of reorder buffer entries using circular carry lookahead	712/224
61	US 4758949 A	☒	Superscalar microprocessor employing a data cache capable of performing store accesses in a single clock cycle	711/3

	Document ID	U	Title	Current OR
62	US 5983342 A	☒	Superscalar microprocessor employing a future file for storing results into multiportion registers	712/218
63	US 5978907 A	☒	Delayed update register for an array	712/239
64	US 5974535 A	☒	Method and system in data processing system of permitting concurrent processing of instructions of a particular type	712/215
65	US 5974240 A	☒	Method and system for buffering condition code data in a data processing system having out-of-order and speculative instruction execution	712/218
66	US 5973712 A	☒	Image recording apparatus	347/188
67	US 5970235 A	☒	Pre-decoded instruction cache and method therefor particularly suitable for variable byte-length instructions	712/213
68	US 5968169 A	☒	Superscalar microprocessor stack structure for judging validity of predicted subroutine return addresses	712/239
69	US 5963973 A	☒	Multiprocessor computer system incorporating method and apparatus for dynamically assigning ownership of changeable data	711/130
70	US 5961634 A	☒	Reorder buffer having a future file for storing speculative instruction execution results	712/218
71	US 5959859 A	☒	Plant monitoring/controlling apparatus	700/2
72	US 5951674 A	☒	Object-code compatible representation of very long instruction word programs	712/210
73	US 5950227 A	☒	CPU write-back cache coherency mechanism that transfers data from a cache memory to a main memory after access of the main memory by an alternative bus master	711/143
74	US 5946468 A	☒	Reorder buffer having an improved future file for storing speculative instruction execution results	712/218
75	US 5941983 A	☒	Out-of-order execution using encoded dependencies between instructions in queues to determine stall values that control issurance of instructions from the queues	712/214
76	US 5935239 A	☒	Parallel mask decoder and method for generating said mask	712/224
77	US 5933618 A	☒	Speculative register storage for storing speculative results corresponding to register updated by a plurality of concurrently recorded instruction	712/217
78	US 5926644 A	☒	Instruction formats/instruction encoding	712/22
79	US 5915110 A	☒	Branch misprediction recovery in a reorder buffer having a future file	712/239
80	US 5913048 A	☒	Dispatching instructions in a processor supporting out-of-order execution	712/215
81	US 5909565 A	☒	Microprocessor system which efficiently shares register data between a main processor and a coprocessor	712/200
82	US 5903741 A	☒	Method of allocating a fixed reorder buffer storage line for execution results regardless of a number of concurrently dispatched instructions	712/218
83	US 5903740 A	☒	Apparatus and method for retiring instructions in excess of the number of accessible write ports	712/217
84	US 5901302 A	☒	Superscalar microprocessor having symmetrical, fixed issue positions each configured to execute a particular subset of instructions	712/215

	Document ID	U	Title	Current OR
85	US 5893154 A	☒	CPU write-back cache coherency mechanism that transeers data from a cache memory to a main memory before access of the main memory by an alternate bus master	711/143
86	US 5892936 A	☒	Speculative register file for storing speculative register states and removing dependencies between instructions utilizing the register	712/216
87	US 5889669 A	☒	Programmable controller allowing an external peripheral device to monitor an internal operation state of a CPU unit	700/17
88	US 5887161 A	☒	Issuing instructions in a processor supporting out-of-order execution	712/244
89	US 5887152 A	☒	Load/store unit with multiple oldest outstanding instruction pointers for completing store and load/store miss instructions	712/217
90	US 5884059 A	☒	Unified multi-function operation scheduler for out-of-order execution in a superscalar processor	712/215
91	US 5881278 A	☒	Return address prediction system which adjusts the contents of return stack storage to enable continued prediction after a mispredicted branch	712/242
92	US 5878255 A	☒	Update unit for providing a delayed update to a branch prediction array	712/240
93	US 5878244 A	☒	Reorder buffer configured to allocate storage capable of storing results corresponding to a maximum number of concurrently receivable instructions regardless of a number of instructions received	712/218
94	US 5875324 A	☒	Superscalar microprocessor which delays update of branch prediction information in response to branch misprediction until a subsequent idle clock	712/238
95	US 5875315 A	☒	Parallel and scalable instruction scanning unit	712/204
96	US 5872951 A	☒	Reorder buffer having a future file for storing speculative instruction execution results	712/218
97	US 5864707 A	☒	Superscalar microprocessor configured to predict return addresses from a return stack storage	712/23
98	US 5860110 A	☒	Conference maintenance method for cache memories in multi-processor system triggered by a predetermined synchronization point and a predetermined condition	711/141
99	US 5860104 A	☒	Data cache which speculatively updates a predicted data cache storage location with store data and subsequently corrects mispredicted updates	711/137
100	US 5859998 A	☒	Hierarchical microcode implementation of floating point instructions for a microprocessor	712/222
101	US 5859991 A	☒	Parallel and scalable method for identifying valid instructions and a superscalar microprocessor including an instruction scanning unit employing the method	712/204
102	US 5857089 A	☒	Floating point stack and exchange instruction	712/222
103	US 5850521 A	☒	Apparatus and method for interprocessor communication	709/208
104	US 5848433 A	☒	Way prediction unit and a method for operating the same	711/137
105	US 5832297 A	☒	Superscalar microprocessor load/store unit employing a unified buffer and separate pointers for load and store operations	710/5
106	US 5832249 A	☒	High performance superscalar alignment unit	712/204

	Document ID	U	Title	Current OR
107	US 5828873 A	☒	Assembly queue for a floating point unit	712/222
108	US 5826071 A	☒	Parallel mask decoder and method for generating said mask	712/224
109	US 5826053 A	☒	Speculative instruction queue and method therefor particularly suitable for variable byte-length instructions	712/210
110	US 5822559 A	☒	Apparatus and method for aligning variable byte-length instructions to a plurality of issue positions	712/214
111	US 5822558 A	☒	Method and apparatus for predecoding variable byte-length instructions within a superscalar microprocessor	712/213
112	US 5819059 A	☒	Predecode unit adapted for variable byte-length instruction set processors and method of operating the same	712/213
113	US 5819057 A	☒	Superscalar microprocessor including an instruction alignment unit with limited dispatch to decode units	712/204
114	US 5816191 A	☒	Stall manager system, module and feeding device for management of mealtimes and food distribution in animal stalls	119/57.92
115	US 5815723 A	☒	Picket autonomy on a SIMD machine	712/20
116	US 5799162 A	☒	Program counter update mechanism	712/205
117	US 5790784 A	☒	Network for time synchronizing a digital information processing system with received digital information	370/520
118	US 5787002 A	☒	Control system for production facilities	700/115
119	US 5781789 A	☒	Superscaler microprocessor employing a parallel mask decoder	712/23
120	US 5768610 A	☒	Lookahead register value generator and a superscalar microprocessor employing same	712/23
121	US 5765221 A	☒	Method and system of addressing which minimize memory utilized to store logical addresses by storing high order bits within a register	711/220
122	US 5764946 A	☒	Superscalar microprocessor employing a way prediction unit to predict the way of an instruction fetch address and to concurrently provide a branch prediction address corresponding to the fetch address	712/239
123	US 5752069 A	☒	Superscalar microprocessor employing away prediction structure	712/23
124	US 5752013 A	☒	Method and apparatus for providing precise fault tracing in a superscalar microprocessor	712/227
125	US 5696955 A	☒	Floating point stack and exchange instruction	712/222
126	US 5694603 A	☒	Computer memory product with preemptive multithreading software	718/107
127	US 5689693 A	☒	Range finding circuit for selecting a consecutive sequence of reorder buffer entries using circular carry lookahead	712/224
128	US 5689672 A	☒	Pre-decoded instruction cache and method therefor particularly suitable for variable byte-length instructions	712/213

	Document ID	U	Title	Current OR
129	US 5678025 A	☒	Cache coherency maintenance of non-cache supporting buses	711/135
130	US 5673418 A	☒	Method and apparatus for emulating the operations of an emulated system terminal driver on a host system	703/23
131	US 5664199 A	☒	Microcomputer free from control of central processing unit (CPU) for receiving and writing instructions into memory independent of and during execution of CPU	710/261
132	US 5655115 A	☒	Processor structure and method for watchpoint of plural simultaneous unresolved branch evaluation	712/239
133	US 5625788 A	☒	Microprocessor with novel instruction for signaling event occurrence and for providing event handling information in response thereto	712/214
134	US 5625415 A	☒	Apparatus and method for automatic focusing in a camera system	348/350
135	US 5617574 A	☒	Devices, systems and methods for conditional instructions	712/200
136	US 5599975 A	☒	Program counter update mechanism	712/230
137	US 5544342 A	☒	System and method for prefetching information in a processing system	711/119
138	US 5539590 A	☒	Floppy disk controller allowed to detect status change of floppy disk driver in standby mode	360/69
139	US 5537602 A	☒	Process system for controlling bus system to communicate data between resource and processor	712/38
140	US 5530888 A	☒	Process and apparatus for controlling a programmable controller with efficient identification of operation completion	710/5
141	US 5517628 A	☒	Computer with instructions that use an address field to select among multiple condition code registers	712/234
142	US 5481685 A	☒	RISC microprocessor architecture implementing fast trap and exception state	712/244
143	US 5481678 A	☒	Data processor including selection mechanism for coupling internal and external request signals to interrupt and DMA controllers	710/22
144	US 5475852 A	☒	Microprocessor implementing single-step or sequential microcode execution while in test mode	714/34
145	US 5448705 A	☒	RISC microprocessor architecture implementing fast trap and exception state	712/244
146	US 5437048 A	☒	Programmable controller acting as a master station and having automatic control of interlock process by using an operation complete address flag	709/208
147	US 5428754 A	☒	Computer system with clock shared between processors executing separate instruction streams	712/220
148	US 5418973 A	☒	Digital computer system with cache controller coordinating both vector and scalar operations	712/3
149	US 5367692 A	☒	Parallel computer system including efficient arrangement for performing communications among processing node to effect an array transposition operation	712/22
150	US 5329630 A	☒	System and method using double-buffer preview mode	711/173
151	US 5321603 A	☒	Programming apparatus for an industrial controller using two-dimensional graphic behavior profiles	700/17

	Document ID	U	Title	Current OR
152	US 5309444 A	☒	Integrated circuit including a test cell for efficiently testing the accuracy of communication signals between a standard cell and an application cell	714/710
153	US 5291581 A	☒	Apparatus and method for synchronization of access to main memory signal groups in a multiprocessor data processing system	711/152
154	US 5286037 A	☒	Electronic hand held logic game	463/9
155	US 5276802 A	☒	Printer control system	385/115
156	US 5251306 A	☒	Apparatus for controlling execution of a program in a computing device	712/217
157	US 5226170 A	☒	Interface between processor and special instruction processor in digital data processing system	712/34
158	US 5226149 A	☒	Self-testing microprocessor with microinstruction substitution	714/25
159	US 5210864 A	☒	Pipelined microprocessor with instruction execution control unit which receives instructions from separate path in test mode for testing instruction execution pipeline	714/37
160	US 5201052 A	☒	System for transferring first and second ring information from program status word register and store buffer	710/260
161	US 5185868 A	☒	Apparatus having hierarchically arranged decoders concurrently decoding instructions and shifting instructions not ready for execution to vacant decoders higher in the hierarchy	712/217
162	US 5159674 A	☒	Method for supplying microcommands to multiple independent functional units having a next microcommand available during execution of a current microcommand	712/207
163	US 5127091 A	☒	System for reducing delay in instruction execution by executing branch instructions in separate processor while dispatching subsequent instructions to primary processor	712/238
164	US 5119483 A	☒	Application of state silos for recovery from memory management exceptions	714/15
165	US 5109329 A	☒	Multiprocessing method and arrangement	710/261
166	US 5093775 A	☒	Microcode control system for digital data processing system	712/212
167	US 5083267 A	☒	Horizontal computer having register multiconnect for execution of an instruction loop with recurrance	712/241
168	US 5042000 A	☒	Integral transform method	708/404
169	US 5038277 A	☒	Adjustable buffer for data communications in a data processing system	710/56
170	US 5036476 A	☒	Printer control system	358/1.18
171	US 5003466 A	☒	Multiprocessing method and arrangement	714/41
172	US 4933941 A	☒	Apparatus and method for testing the operation of a central processing unit of a data processing system	714/31
173	US 4872106 A	☒	Industrial process control system with back-up data processors to take over from failed primary data processors	714/13

	Document ID	U	Title	Current OR
174	US 4860244 A	☒	Buffer system for input/output portion of digital data processing system	711/219
175	US 4831520 A	☒	Bus interface circuit for digital data processor	710/305
176	US 4742451 A	☒	Instruction prefetch system for conditional branch instruction for central processor unit	712/235
177	US 4740893 A	☒	Method for reducing the time for switching between programs	712/222
178	US 4718759 A	☒	Apparatus for the alignment and balance of the wheels of a motor vehicle	356/139.09
179	US 4700330 A	☒	Memory for a digital data processing system including circuit for controlling refresh operations during power-up and power-down conditions	365/222
180	US 4604750 A	☒	Pipeline error correction	714/764
181	US 4583222 A	☒	Method and apparatus for self-testing of floating point accelerator processors	714/40
182	US 4553201 A	☒	Decoupling apparatus for verification of a processor independent from an associated data processing system	714/46
183	US 4527247 A	☒	Environmental control system	700/278
184	US 4527237 A	☒	Data processing system	709/253
185	US 4519027 A	☒	Industrial control, communications and information system	700/80
186	US 4516199 A	☒	Data processing system	710/20
187	US 4488258 A	☒	Programmable controller with control program comments	700/18
188	US 4486849 A	☒	Computer for calculating compound interest	708/134
189	US 4413319 A	☒	Programmable controller for executing block transfer with remote I/O interface racks	710/30
190	US 4394725 A	☒	Apparatus and method for transferring information units between processes in a multiprocessing system	718/106
191	US 4378588 A	☒	Buffer control for a data path system	710/57
192	US 4374409 A	☒	Method of and system using P and V instructions on semaphores for transferring data among processes in a multiprocessing system	718/106
193	US 4354225 A	☒	Intelligent main store for data processing systems	711/5
194	US 4325119 A	☒	Process and apparatus employing microprogrammed control commands for transferring information between a control processor and communications channels	710/5
195	US 4322846 A	☒	Self-evaluation system for determining the operational integrity of a data processing system	714/46
196	US 4320451 A	☒	Extended semaphore architecture	718/106

	Document ID	U	Title	Current OR
197	US 4318182 A	☒	Deadlock detection and prevention mechanism for a computer system	718/105
198	US 4316245 A	☒	Apparatus and method for semaphore initialization in a multiprocessing computer system for process synchronization	718/106
199	US 4313161 A	☒	Shared storage for multiple processor systems	711/151
200	US 4308959 A	☐	Roll sorting apparatus	209/563